Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1CLR**
2. **1J**
3. **1N.K**
4. **1CK**
5. **1PR**
6. **1Q**
7. **1N.Q**
8. **GND**
9. **2N.Q**
10. **2Q**
11. **2PR**
12. **2CK**
13. **2N.K**
14. **2J**
15. **2CLR**
16. **VCC**

**3**

**4**

**5**

**6 7 8 9 10**

**13**

**12**

**11**

**2 1 16 15 14**

**LS**

**109**

**B**

**MASK REF**

**.051”**

**.048”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: LS 109 B**

**APPROVED BY: DK DIE SIZE .048” X .051” DATE: 7/1/16**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: 54LS109**

**DG 10.1.2**

#### Rev B, 7/19/02